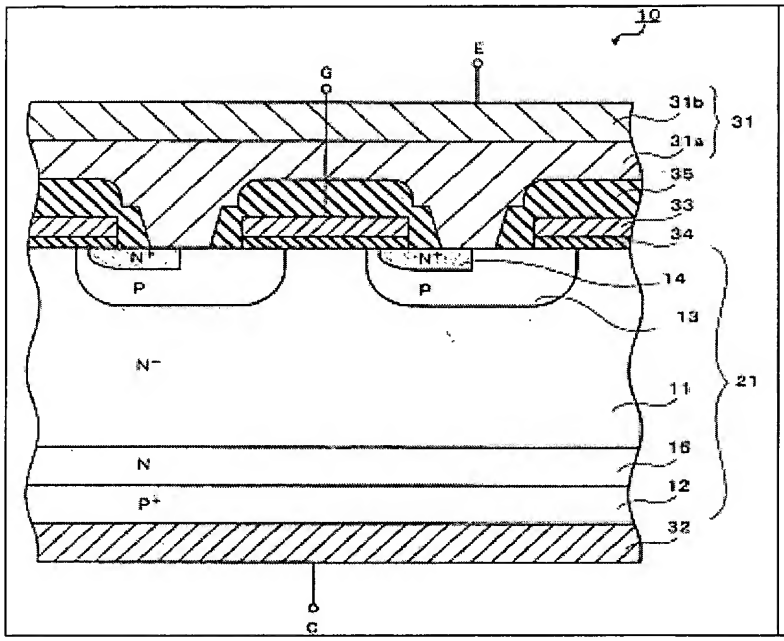
REMARKS/ARGUMENTS

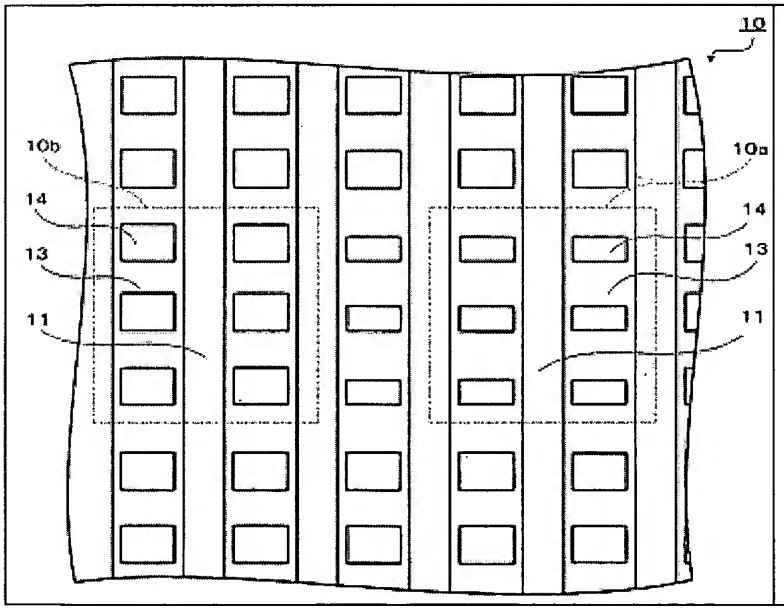
Claims 1 and 3-4 are amended by this response. No claims are canceled or added. Accordingly, upon entry of these amendments and remarks, Claims 1-4 will remain pending.

Embodiments of the present invention relate to semiconductor devices. FIG. 3 (reproduced below), shows a cross-sectional view of one device formed in a substrate (21):



- first semiconductor region (11) has a first conductivity type,
- second semiconductor regions (13) having a second conductivity type are formed in a specific surface portions of said first semiconductor region (11), and
- third semiconductor region (14) having the first conductivity type is formed in a specific surface portion of said second semiconductor regions (13)

FIG. 3 shows a corresponding plan view of the arrangement of a plurality of such devices in the substrate, with overlying layers 31, and 33-35 omitted:



- first region (10a) in which one of said third semiconductor regions (14) is formed at a center of said semiconductor base (11)
- second region (10b) in which another of said third semiconductor regions (14) is formed at a circumference of said semiconductor base (11) so as to enclose said one of first regions (10a)
- third semiconductor regions (14) in said first region 10a, have a surface area larger than that of third semiconductor regions (14) in said second region (10b)

As described in the specification at least at ¶[0039], such a configuration reduces the likelihood of occurrence of an undesirable thermal runaway effect.

Accordingly, claim 1 has now been amended to recite:

> 1. A semiconductor device, comprising:
> a semiconductor base comprising a plurality of first semiconductor regions having a first conductivity type, a plurality of second semiconductor regions having a second conductivity type formed in a specific surface portion of said first semiconductor regions, and a plurality of third semiconductor regions having the first conductivity type formed in a specific surface portion of said second semiconductor regions; and
> a first electrode formed directly above said second semiconductor region that is between said first semiconductor region and said third semiconductor regions,
> wherein: a first region, in which one of said third semiconductor regions exhibiting a first surface area, is formed at a center of said semiconductor base, and
> a second region, in which another of said third semiconductor regions exhibits a second surface area larger than said first surface area, is formed at a circumference of said semiconductor base so as to enclose said first region.

In summary, embodiments of the present invention include structures:

(a) Having first and second regions. The ratio by which a third semiconductor region occupies an area of the first region is different from the ratio by which the third semiconductor region occupies an area of the second region.

(b) The ratio (of area) by which the third semiconductor region occupies the second region is larger than the ratio (of area) by which the third region occupies the first region.

(c) The first region is formed in the center part of the semiconductor base, and the second region is formed in the periphery of the semiconductor substrate so as to surround the first region.

In the latest office action, the Examiner rejected claims 1-4 as purportedly failing to comply with the written description requirement. Claim 1 is now amended as indicated above, in the manner suggested by the Examiner, to overcome these claim rejections.

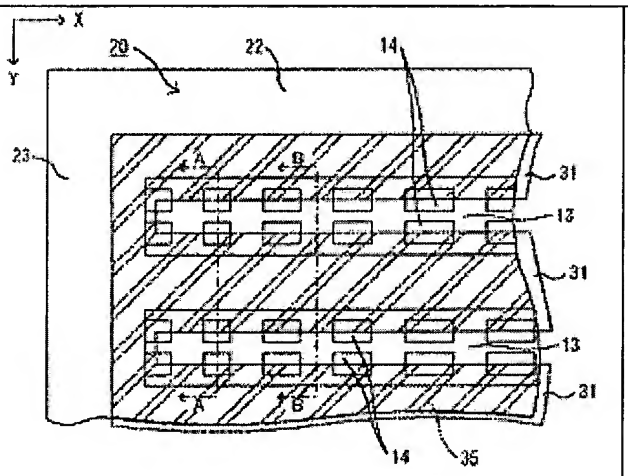
Also in the latest office action, the Examiner rejected claims 1-4 as purportedly being indefinite. Claim 1 is also amended as indicated above, in a manner calculated to overcome these indefiniteness claim rejections.

Turning now to address rejection of the claims in view of alleged prior art, claims 1-4 stand rejected as anticipated by JP Patent Application Publication No. 2004-228553 to Torii et al. ("the Torii Publication"). It is noted that the claims stand rejected as anticipated, and not merely obvious, in view of the Torii Publication:

> for anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. (Emphasis added; MPEP 706.2)

Here, Applicants were unable to locate teaching regarding a second region formed in a periphery of a substrate such that it encloses a first region formed in a central region of a substrate.

In relying upon the Torii Publication to reject the claims, the Examiner relied upon FIG. 1(b) (reproduced below) to make the following correlations with the claim elements:



- the second region (14) from the left in the second row, purportedly corresponds to the first region;
- the first region (14) from the right in the bottom row, purportedly corresponds to the second region.

It is respectfully asserted that the wording of the amended independent claim 1 now sufficiently distinguishes the Torii Publication. In particular, the device of the Torii Publication is formed so that the further the position of each emitter region is from the trunk of the bus line in the direction in which the p-type base region extends, the larger the area of the emitter region (or vice versa).

On the other hand, the direction perpendicular to the direction in which the p-type base region extends, the area of each emitter region is the same in both sides close to the trunk and close to the edge of the semiconductor substrate. Thus in the Torii Publication, the areas of emitter regions vary solely in the direction in which the p-type base region extends.

Therefore, the semiconductor device of the cited reference is susceptible to thermal runaway caused by heat generated in the peripheral portion of the device and transmitted to the center part thereof or to having an insufficient amount of current secured in the peripheral part causing a decrease of current capacity for the entire semiconductor device.

In contrast, in embodiments of the present invention, the area of each emitter region in the side close to the center of the semiconductor substrate (a first region) is different from the

area of each emitter region in the side close to the periphery of the semiconductor substrate (a second region). That is, according to embodiments of the present invention, the area of each emitter region in the center part of the semiconductor substrate is different from the area of each emitter region in the peripheral part of the semiconductor substrate (i.e. in directions that include the direction in which a p-type region extends, and the direction orthogonal to that direction).

Therefore, a sufficient amount of current is secured in the periphery of the semiconductor substrate so that the current capacitance of the entire semiconductor device is not suppressed. Furthermore, the amount of current flowing in the center part is smaller than the amount of the current flowing in the peripheral part. This generates less heat in the center part than in the peripheral part.

Based upon the failure of the art being relied upon, to teach explicitly or even impliedly, all of the elements of the claims, it is respectfully asserted that the claims cannot be considered anticipated by that reference. Continued maintenance of these claim rejections is improper, and the claim rejections have been overcome.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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